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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,016	02/10/2004	Yoon-Jong Song	5649-1257	9795

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EXAMINER	
TRAN, THIEN F	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/775,016	SONG ET AL.
	Examiner	Art Unit
	Thien F. Tran	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-17 and 20-30* is/are rejected.

7)☒ Claim(s) *6,18 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/04/05, 02/10/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-30 in the reply filed on 01/28/2005 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 7-11 and 23-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoshikawa et al. (USPN 6,717,198).

Yoshikawa et al. discloses the claimed ferroelectric memory device (Figures 2, 3), comprising: a semiconductor substrate 100 having a transistor; a lower portion of interlayer film 105 characterized as a first interlayer dielectric on the semiconductor substrate that surrounds a gate electrode 102 of the transistor; a plug 106 penetrating the first interlayer dielectric; a capacitor electrically connected to the plug, the capacitor having a bottom electrode that has a top surface and a plurality of side surfaces, a capacitor-ferroelectric layer 112 and a top electrode113; and a reaction buffer layer 111 between the first interlayer dielectric and the capacitor-ferroelectric layer.

Regarding claim 2, the reaction buffer layer 111 is adjacent to the side surfaces of the bottom electrode, and a top surface of the reaction buffer layer and the top surface of the bottom electrode form a planar surface.

Regarding claims 3 and 25, Yoshikawa et al. further discloses the device comprising a third interlayer dielectric(an upper portion of layer 105) on the first interlayer dielectric (a lower portion of layer 105) and under the reaction buffer layer 111, and wherein the reaction buffer layer comprises a material that prevents a reaction between the third interlayer dielectric and the capacitor-ferroelectric layer.

Regarding claims 4 and 26, the reaction buffer layer comprises a material (titanium oxide or aluminum oxide).

Regarding claim 5, the device further comprises a bit line 117 that is electrically connected to the transistor on the first interlayer dielectric; and a lower portion of layer 116 between two adjacent layer 111 characterized as a third interlayer dielectric recessed between the bottom electrode and a second bottom electrode associated with a capacitor of an adjacent ferroelectric memory device (see Figure 2).

Regarding claim 7, the device further comprises a second interlayer dielectric (an upper portion of the interlayer film 105) between the first interlayer dielectric (the lower portion of the interlayer film 105) and the third interlayer dielectric 116, wherein the plug 106 further penetrates the second interlayer dielectric to electrically connect the bottom electrode to the semiconductor substrate.

Regarding claim 8 and 9, the device further comprises an oxygen diffusion barrier 111 on the first interlayer dielectric 105 and side surfaces of the bottom electrode 109.

Regarding claims 10-11 and 27-28, the bottom electrode 109 is made from the multilayer film of iridium film, iridium oxide film and platinum film wherein the iridium film inherently serves as an oxygen diffusion barrier, the iridium oxide inherently provides the ferroelectric layer with oxygen, and the platinum film inherently has a lattice point that allows for formation of a ferroelectric layer having a crystalline structure.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 12-17 and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikawa et al. (USPN 6,717,198) in view of Gilbert et al. (USPN 6,709,875).

Yoshikawa et al. as described above does not specifically disclose the top electrode 113 comprising iridium oxide as a fourth material and iridium as a fifth material. Gilbert et al. discloses a top electrode 16 of a ferroelectric capacitor comprising iridium oxide and iridium conductive layers. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to form the top electrode 113 comprising iridium oxide as a fourth material and iridium as a fifth material

as taught by Gilbert et al. in order to absorb oxygen without impairing the conductivity of the top electrode.

Regarding claims 12 and 29, the fourth material of iridium oxide in top electrode 113 inherently provides the ferroelectric layer with oxygen and the fifth material of iridium inherently improves the strength of the fourth material.

Regarding claims 15-17, Yoshikawa et al. discloses a hydrogen diffusion barrier 115 of aluminum oxide on the capacitor-ferroelectric layer 112 and on the top electrode 113.

Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikawa et al. (USPN 6,717,198) in view of Chien et al. (USPN 6,406,971).

Yoshikawa et al. as described above does not disclose a first contact pad between the bit line and the semiconductor substrate and a second contact pad between the plug and the semiconductor substrate. Chien et al. discloses a first polysilicon contact pad 238 between the bit line and the semiconductor substrate and a second polysilicon contact pad 240 between the plug and the semiconductor substrate as shown in Figure 2F. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate a first polysilicon contact pad between the bit line and the semiconductor substrate and a second polysilicon contact pad between the plug and the semiconductor substrate of Yoshikawa et al. so that minor misalignment of the plugs on the wide surface areas of the contact pads does not present a problem.

Allowable Subject Matter

Claims 6, 18 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: prior art references do not teach or render obvious a ferroelectric memory device comprising a third interlayer dielectric recessed between a bottom electrode and a second bottom electrode wherein the reaction buffer layer is on the third interlayer dielectric.

Prior art references do not teach or render obvious a ferroelectric memory device having the structure with claimed features arranged as recited in claim 18.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien F. Tran whose telephone number is (571) 272-1665. The examiner can normally be reached on 8:30AM - 5:00PM Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tt
April 15, 2005

Thien Tran

THIEN TRAN
PRIMARY EXAMINER